



Memory Map

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=====
$0000 - $007F CPU internal RAM
$2000 - $27FF 6116 Static RAM
$4000 - $400F 6522 VIA registers
$6000 - $7FFF 2764 EPROM

(Imaged memory regions)
$A000 - $A7FF 6116 Static RAM
$C000 - $C00F 6522 VIA registers
$E000 - $FFFF 2764 EPROM
  
```

6522 VIA Register Mapping

Since the address lines to this chip are wired backward then the register layout differs according to the datasheet. Register names acquired from 6522 VIA Datasheet (2000)

| | | | |
|---------------|---------------|---------------|----------------|
| \$4000 - ORB | \$4004 - DDRB | \$4008 - ORA | \$400C - DDRA |
| \$4001 - T2CL | \$4005 - SR | \$4009 - T2CH | \$400D - ACR |
| \$4002 - T1CL | \$4006 - T1LL | \$400A - T1CH | \$400E - T1LH |
| \$4003 - PCR | \$4007 - IER | \$400B - IFR | \$400F - ORANO |

Original circuit created by Peter Ihnat
Electronics Today International Australia
April 1984, Page 65 to 69.

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|---|--------------------|---------------|
| Title | | |
| ETI-662a General Purpose Microprocessor System | | |
| Size | Number | Revision |
| A4 | C662 | EA |
| Date: | 13-May-2002 | Sheet 1 of 1 |
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